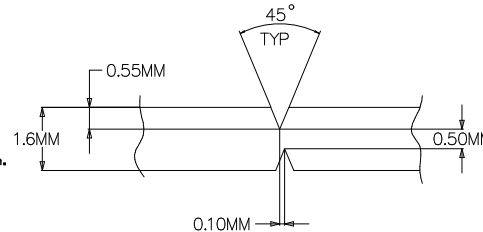


Symbol	Count	Hole Size	Plated	Hole Length	Hole Tolerance
E	12	7.87mil (0.200mm)	PTH	-	+/-3.00mil
▽	1224	8.00mil (0.203mm)	PTH	-	+/-3.00mil
⊗	3	23.62mil (0.600mm)	PTH	-	+/-3.00mil
■	4	23.62mil (0.600mm)	PTH	51.18mil (1.300mm)	+/-3.00mil
⊗	2	33.47mil (0.850mm)	NPTH	-	+/-3.00mil
◇	4	33.47mil (0.850mm)	PTH	-	+/-3.00mil
⊗	16	39.37mil (1.000mm)	PTH	-	+/-3.00mil
✕	2	39.37mil (1.000mm)	PTH	118.11mil (3.000mm)	+/-3.94mil
⊗	1	39.37mil (1.000mm)	PTH	137.79mil (3.500mm)	+/-3.94mil
⊗	1	40.00mil (1.016mm)	PTH	-	+/-3.00mil
⊗	2	40.16mil (1.020mm)	NPTH	-	+/-2.00mil
B	7	40.16mil (1.020mm)	PTH	-	+/-3.00mil
⊗	4	43.31mil (1.100mm)	PTH	-	+/-3.00mil
⊗	6	49.21mil (1.250mm)	PTH	-	+/-3.00mil
⊗	3	118.11mil (3.000mm)	NPTH	-	+/-2.00mil
□	4	118.11mil (3.000mm)	PTH	-	+/-3.00mil
▽	4	160.00mil (4.064mm)	NPTH	-	+/-2.00mil
1299 Total					

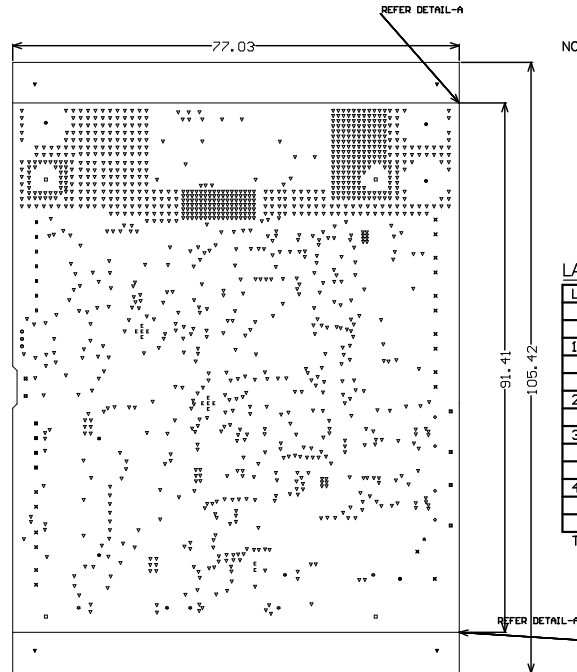
Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

IMPEDANCE TABLE

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	4.5 MILS	4.5 MILS	90 OHM	LAYER-2
BOTTOM	4.5 MILS	4.5 MILS	90 OHM	LAYER-3
TOP / BOTTOM	5.9 MILS	-	50 OHM	LAYER-2 / LAYER-3
TOP	4 MILS	6 MILS	100 OHM	LAYER-2
TOP	4 MILS	5.1 MILS	120 OHM	LAYER-3



DETAIL-A(V-GROOVE DETAILS)
SCALE : NTS



NOTES : UNLESS OTHERWISE SPECIFIED.

1. ALL VIAS ARE TIENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
2. ALL VIAS SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT.
3. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. BOARD DIMENSIONS ARE IN MM.
5. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIAS AND THROUGH HOLE PADS.
6. ALL UNCONNECTED VIAS SHALL BE SUPPRESSED.

LAYER STACK-UP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		1.85mil		
	Dielectric 1	Iteq IT180A Prepreg 106 RC71-NEW	1.78mil	3.79	
	Dielectric 2	Iteq IT180A Prepreg 106 RC71-NEW	1.78mil	3.79	
2	L2_GND1		1.26mil		
	Dielectric 3	Iteq IT180A 50 mil core I/I	47.24mil	4.28	
3	L3_PWR1		1.26mil		
	Dielectric 4	Iteq IT180A Prepreg 106 RC71-NEW	1.78mil	3.79	
	Dielectric 5	Iteq IT180A Prepreg 106 RC71-NEW	1.78mil	3.79	
4	Bottom Layer		1.85mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Total board thickness: 62.58mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 4.0 MIL
MIN. CLEARANCE: 4.5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.127mm (5.0MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- .2 MIL HOLES +/- .3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- .3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☐ MATTIE ☒ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ ALL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☒ BOARD IMPEDANCE SHALL BE FOLLOWED AS PER THE
IMPEDANCE SPECIFICATION TABLE.



PROJECT TITLE:
BP-IWRL6432WMOD

DESIGNED FOR:
Public Release

FILE NAME:
PROC212A_PCB.PcbDoc

ENGINEER:
Mistral

LAYOUT BY:
Mistral

SCALE: 1.62

ALTUM DESIGNER VERSION:
22.11.1.43

ALL ARTWORK VIEWED FROM TOP SIDE

BOARD #: PROC212

REV: A

SUN REV: Not in version control

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LAYER NAME = Drill Dwg@image
MI Board Outline

TID #: N/A

PLOT NAME = FAB PDF

GENERATED : 15-10-2025 11:58:43

TEXAS INSTRUMENTS